Typical Specifications for PLCRO in 0.5 to 3.2 GHz range				
Available Models	**NXLFHP**	**NXLFLC**	**NXLFI**	**NXLFDL**
Any fixed frequency (GHz) in the range of	0.5 to 3			
Frequency Stability (ppm, over temp)	N/A (1)	N/A (1)	+/- 5 std,0.1 option (4)	N/A (1)
Frequency Accuracy (ppm)	0	0.1 (3)	0.1	0.1 (3)
Output Power in dBm (over temp)	> +13 standard, up to +23 dBm avail			
Power variation in dB (over temp)	< 2.0			
Pulling (1.5:1 VSWR)	Will not break lock			
Harmonics in dBc (typ)	< - 20 standard, -40 option			
Discrete Spurious in dBc	< - 80, levels to -100 dBc option			
External Reference Frequency (standard)	50,100 MHz	5,10 MHz	N/A	5,10 MHz
External Reference Input Power (2)	0+/- 3 dBm	10+/- 3 dBm	N/A	0+/- 3 dBm
Phase Lock Alarm (also TTL, CMOS levels)	Open Collector (locked=open, unlocked=ground)-			
Operating Temperature ranges	0 to 60^{o}C, -20 to 70^{o}C, -40 to 85^{o}C, -55 to 85^{o}C			
Power Supply (Vdc, +8V, 15V, 24V option)	+12			
DC Current Draw	250	80	400	400
RF Connector (2 places)	SMA Female (Field replaceable option available)			
DC Connectors	Solder pin			
Size: Length X Width Height (inches)	2.25 X 2.25X0.63	2.25 X 2.25X0.63	2.25 X 2.25X1.48	2.25 X 2.25X1.48
Outline (5)	DC200102 Rev 4C	DC200102 Rev 4C	DC200106 Rev 2I	DC200106 Rev 2G
Weight (in ounces):	4.5	4.5	8.0	8.0

(1) coherent to external reference
(2) Input power levels from -20 to +10 dBm +/- 3 dBm option
(3) Output frequency may be specified to nearest 100 Hz regardless of ext ref freq.
(4) as low as +/-0.05ppm stability over -40 to +85C available
(5) outline drawing quoted may vary depending on specs and price considerations

NXLFHP = High Performance Single Loop PLCRO, ext ref ~ 100 MHz				
Phase Noise in dBc/Hz vs offset vs output freq	800 MHz	1200 MHz	2000 MHz	2800 MHz
100 Hz	-105	-100	-98	-96
1 KHz	-120	-117	-115	-115
10 KHz	-132	-130	-129	-125
100 KHz	-138	-135	-135	-132
1 MHz	-150	-150	-150	-150
Note: Guaranteed phase noise specs will be 5 dB worse than typical				
End User Phase Noise dependent on external reference phase noise for F offset < 100 kHz				

NXLFLC = Low Cost Single Loop PLCRO, 5 or 10 MHz external reference				
Phase Noise in dBc/Hz vs offset vs output freq	800 MHz	1200 MHz	2000 MHz	2800 MHz
10 KHz	-120	-115	-113	-108
100 KHz	-135	-135	-133	-128
1 MHz	-150	-150	-150	-150
Note: Guaranteed phase noise specs will be 5 dB worse than typical				
End User Phase Noise dependent on external reference phase noise for F offset < 2 kHz				

NXLFI = High Performance Single Loop PLCRO with internal OCXO reference				
Phase Noise vs offset vs output freq (dBc/Hz)	800 MHz	1200 MHz	2000 MHz	2800 MHz
100 Hz	-103	-98	-95	-94
1 KHz	-120	-117	-116	-115
10 KHz	-132	-130	-129	-127
100 KHz	-138	-135	-135	-132
1 MHz	-150	-150	-150	-150
Note: Guaranteed phase noise specs will be 5 dB worse than typical				
Guaranteed Phase Noise @ 100, 1kHz may be worse by 10 dB unless user specifies ULN option				

NXLFDL = High Performance Dual Loop -consists of PLCRO driven by PLXO w 5 to 10 MHz external reference				
Phase Noise in dBc/Hz vs offset vs output freq	800 MHz	1200 MHz	2000 MHz	2800 MHz
100 Hz	-103	-98	-95	-94
1 KHz	-120	-117	-116	-115
10 KHz	-132	-130	-129	-127
100 KHz	-138	-135	-135	-132
1 MHz	-150	-150	-150	-150
Note: Guaranteed phase noise specs will be 5 dB worse than typical				
Guaranteed Phase Noise @ 100, 1kHz may be worse by 10 dB unless user specifies ULN option				

Typical Specifications for PLDRO in 3 to 16.5 GHz range			
Available Models	**NXPLOS**	**NXPLOS-I**	**NXPLOS-DL**
Any fixed frequency (GHz) in the range of	3 to 16.5 GHz		
Frequency Stability (+/- ppm, over temp)	N/A (1)	5 std, 0.5, 0.1 (4)	N/A (1)
Frequency Accuracy (+/- ppm @ 25C)	0	0.1	0 std, 0.1 (3)
Output Power in dBm (over temp)	> +15 standard, up to +20 dBm avail		
Power variation in dB (over temp)	< 3		
Pulling (1.5:1 VSWR)	Will not break lock		
Harmonics in dBc (typ)	< - 20		
Discrete Spurious in dBc	< - 80, levels to -100 dBc avail.		
External Reference Frequency (standard)	50,100 MHz	N/A	5,10 MHz
External Reference Input Power (2)	0+/- 3 dBm	N/A	0+/- 3 dBm
Phase Lock Alarm (also TTL, CMOS levels)	Open Collector (locked=open, unlocked=ground)-		
Operating Temperature ranges	0 to 60^{o}C, -20 to 70^{o}C, -40 to 85^{o}C, -55 to 85^{o}C		
Power Supply (Vdc, +8V, 15V, 24V option)	+12		
DC Current Draw	270	400	400
RF Connector (2 places)	SMA Female (Field replaceable option available)		
DC Connectors	Solder pin		
Size: Length X Width Height (inches)	2.25 X 2.25X0.63	2.25 X 2.25X1.48	2.25 X 2.25X1.48
Outline Fout> 6 GHz (5)	DC200102 Rev 15	DC200106 Rev 2B	DC200106 Rev 2C
Outline Fout< 6 GHz (5)	DC200102 Rev 8	DC200106 Rev 2F	DC200106 Rev 2E
Weight (in ounces):	4.5	8.0	8.0

(1) coherent to external reference
(2) Input power levels from -20 to +10 dBm +/- 3 dBm option
(3) Output frequency may be specified to nearest 1000 Hz regardless of external reference frequency
(4) standard is +/-5 ppm, as low as +/-0.05 ppm stability over -40 to +85C available
(5) Standard outline is thicker by 0.125" below 6 GHz

NXPLOS = Single Loop PLDRO, ext ref ~ 100 MHz								
Phase Noise in dBc/Hz vs offset vs output freq in GHz	3.90	5.20	6.80	9.20	10.50	12.00	14.00	16.00
100 Hz	-97	-96	-93	-91	-90	-88	-87	-86
1 KHz	-120	-119	-116	-114	-113	-111	-110	-109
10 KHz	-128	-125	-124	-121	-120	-117	-114	-113
100 KHz	-131	-128	-127	-125	-123	-122	-119	-117
1 MHz	-148	-147	-146	-144	-142	-138	-136	-135
Note: Guaranteed phase noise specs will be 5 dB worse than typical.								
End User Phase Noise dependent on external reference phase noise for F offset < 100 kHz								

NXPLOS-I = Single Loop PLDRO with internal OCXO w LN option								
Phase Noise in dBc/Hz vs offset vs output freq in GHz	3.90	5.20	6.80	9.20	10.50	12.00	14.00	16.00
100 Hz	-95	-93	-90	-88	-87	-85	-84	-83
1 KHz	-119	-116	-113	-111	-110	-108	-107	-106
10 KHz	-128	-125	-124	-121	-120	-117	-114	-112
100 KHz	-131	-128	-127	-125	-123	-122	-119	-116
1 MHz	-148	-147	-146	-144	-142	-138	-136	-135
Note: Guaranteed phase noise specs will be 5 dB worse than typical								
Guaranteed Phase Noise @ 100, 1kHz may be worse by 10 dB unless user specifies LN option								

NXPLOS-DL = Dual Loop consisting of PLDRO driven by PLXO with 10 MHz external reference w LN option								
Phase Noise in dBc/Hz vs offset vs output freq in GHz	3.90	5.20	6.80	9.20	10.50	12.00	14.00	16.00
100 Hz	-95	-93	-90	-88	-87	-85	-84	-83
1 KHz	-119	-116	-113	-111	-110	-108	-107	-106
10 KHz	-128	-125	-124	-121	-120	-117	-114	-112
100 KHz	-131	-128	-127	-125	-123	-122	-119	-116
1 MHz	-148	-147	-146	-144	-142	-138	-136	-135
Note: Guaranteed phase noise specs will be 5 dB worse than typical								
Guaranteed Phase Noise @ 100, 1kHz may be worse by 10 dB unless user specifies LN option								

Phase Noise specs for I and DL models assume use of 100 MHz crystal oscillator with phase of	
100 Hz	< - 127
1 KHz	< - 150
10 KHz	< - 165
100 KHz	< - 165

Typical Specifications for PLDRO in 16.5 to 30 GHz range			
Available Models	**NXPLOS**	**NXPLOS-I**	**NXPLOS-DL**
Any fixed frequency (GHz) in the range of	16.5 to 30 GHz		
Frequency Stability (+/- ppm, over temp)	N/A (1)	5 std, 0.5, 0.1 (4)	N/A (1)
Frequency Accuracy (+/- ppm)	0	0.1	0 std, 0.1 (3)
Output Power (dBm, over temp)	> +13 standard, up to +20 dBm option		
Power variation (dBm, over temp)	< 3		
Pulling (1.5:1 VSWR)	Will not break lock		
Harmonics (dBc)	< - 20		
Subharmonics dBc (N*Fout/2, N odd)	< - 20 standard, - 45 option		
Discrete Spurious in dBc	< - 70 standard, - 85 option		
External Reference Frequency (standard)	50,100 MHz (5)	N/A	5,10 MHz
External Reference Input Power (2)	0+/- 3 dBm	N/A	0+/- 3 dBm
Phase Lock Alarm (also TTL, CMOS levels)	Open Collector (locked=open, unlocked=ground)-		
Operating Temperature ranges	0 to 60^{o}C, -20 to 70^{o}C, -40 to 85^{o}C, -55 to 85^{o}C		
Power Supply (Vdc, +8V, 15V, 24V option)	+12		
DC Current Draw	350	550	550
RF Connector (2 places)	SMA Female (Field replaceable option available)		
DC Connectors	Solder pin		
Size: Length X Width Height (inches)	2.25" X 2.25" X 0.63"	2.25" X 2.25" X 1.48"	2.25" X 2.25" X 1.48"
Outline Drawing	DC200102 Rev 15	DC200106 Rev 2B	DC200106 Rev 2C
Weight (in ounces):	4.5	8.0	8.0

(1) coherent to external reference
(2) Input power levels from -20 to +10 dBm +/- 3 dBm option
(3) Output frequency may be specified to nearest 1000 Hz regardless of external reference frequency
(4) standard is +/-5 ppm, as low as +/-0.05 ppm stability over -40 to +85C available
(5) RF Output Frequency MUST be a multiple of twice the reference frequency

NXPLOS = Single Loop PLDRO, ext ref ~ 100 MHz					
Phase Noise in dBc/Hz vs offset vs output freq in GHz	18.00	20.00	22.00	24.00	26.00
100 Hz	-85	-84	-83	-82	-82
1 KHz	-107	-106	-105	-104	-104
10 KHz	-113	-113	-112	-110	-107
100 KHz	-115	-115	-114	-112	-110
1 MHz	-130	-130	-128	-127	-125
Note: Guaranteed phase noise specs will be 5 dB worse than typical					
End User Phase Noise dependent on external reference phase noise for F offset < 100 kHz					

NXPLOS-I = Single Loop PLDRO with internal OCXO					
Phase Noise in dBc/Hz vs offset vs output freq in GHz	18.00	20.00	22.00	24.00	26.00
100 Hz	-82	-81	-80	-79	-79
1 KHz	-104	-103	-102	-101	-101
10 KHz	-113	-113	-112	-110	-107
100 KHz	-115	-115	-114	-112	-110
1 MHz	-130	-130	-128	-127	-125
Note: Guaranteed phase noise specs will be 5 dB worse than typical					
Guaranteed Phase Noise @ 100, 1kHz may be worse by 10 dB unless user specifies LN option					

NXPLOS-DL = Dual Loop consisting of PLDRO driven by PLXO with 5 or 10 MHz external reference					
Phase Noise in dBc/Hz vs offset vs output freq in GHz	18.00	20.00	22.00	24.00	26.00
100 Hz	-82	-81	-80	-79	-79
1 KHz	-104	-103	-102	-101	-101
10 KHz	-113	-113	-112	-110	-107
100 KHz	-115	-115	-114	-112	-110
1 MHz	-130	-130	-128	-127	-125
Note: Guaranteed phase noise specs will be 5 dB worse than typical					
Guaranteed Phase Noise @ 100, 1kHz may be worse by 10 dB unless user specifies LN option					

Phase Noise specs for I and DL models assume use of 100 MHz crystal oscillator with phase of	
100 Hz	< - 127
1 KHz	< - 149
10 KHz	< - 165
100 KHz	< - 165